

What is Claimed is:

1 1. During the testing of the operation of processing
2 unit, a system for identifying the occurrence of a
3 processor unit debug halt condition, the system comprising:
4 timing trace apparatus responsive to signals from the
5 processor unit, the timing trace apparatus generating a
6 timing trace stream;

7 program counter trace apparatus responsive to signals
8 from the processing unit, the program counter trace
9 apparatus generating a program counter trace stream; and

10 synchronization apparatus applying periodic signals to
11 the timing trace apparatus and to the program counter trace
12 apparatus, the periodic signals providing a synchronization
13 between trace streams;

14 wherein the program counter trace apparatus is
15 responsive to a debug halt signal, the program counter
16 trace apparatus generating marker signal group identifying
17 the occurrence of the debug halt signal and relating the
18 debug halt signal to the timing trace stream.

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20 2. The system as recited in claim 1 wherein the
21 marker signal group includes a program counter address, a
22 timing index and a periodic sync ID.

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24 3. The system as recited in claim 1 further
25 comprising:

1 data trace apparatus responsive to signals from the
2 processing unit, the data trace apparatus generating a data
3 trace stream, wherein the periodic signals are applied to
4 the data trace apparatus; and

5 a host processing unit, the host processing unit
6 responsive to the timing trace stream, the program counter
7 trace stream and the data trace stream, the host processing
8 unit reconstruction the processing activity of the
9 processing unit from the trace streams.

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11 4. The method for communicating an occurrence of a
12 debug halt signal from a target processor unit to a host
13 processing unit, the method comprising:

14 generating a timing trace stream, a program counter
15 trace stream, and data trace stream, and

16 in the program counter trace stream, including a
17 marker signal group indicating an occurrence of debug halt
18 signal and relating the occurrence of the debug halt signal
19 to the data trace stream and to the timing trace stream.

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21 5. The method as recited in claim 4 further
22 comprising:

23 in the marker signal group, including a periodic sync
24 ID, a timing index and a program counter address.

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26 6. In a processing unit test environment wherein a
27 target processor transmits a plurality of trace streams to

1 a host processing unit, a marker signal group included in a
2 trace signal stream, the marker signal group comprising:
3 indicia of the occurrence of a debug halt signal;
4 indicia of the relationship of the occurrence of the
5 debug halt signal to the target processor clock; and
6 indicia of the relationship of the occurrence of the
7 debug halt signal to the target processor program
8 execution.

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10 7. In a target processing unit generating trace test
11 signals for transfer to a host processing unit, program
12 counter trace generation apparatus comprising:

13 a storage unit;

14 a decoder unit responsive to a rest signal for storing
15 a signal group identifying the debug halt signal in the
16 storage unit in a first location in the storage unit, the
17 decoder unit generating a control signal;

18 a gate unit responsive to the control signal, the gate
19 unit transmitting processor signals applied thereto to the
20 storage unit for storage at defined locations, the signals
21 stored in the storage unit forming a debug halt sync
22 marker; and

23 a FIFO unit coupled to the storage unit, the FIFO unit
24 receiving the debug halt sync marker when the debug halt
25 marker is complete, the FIFO unit transferring the debug
26 halt sync marker to the host processing unit.

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1 8. The program counter trace apparatus as recited in
2 claim 7 responsive to a selected control signal for
3 transferring debug halt sync marker in the FIFO unit to an
4 output port of the target processor.

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6 9. The program counter trace apparatus as recited in
7 claim 10 wherein the debug halt sync marker signal includes
8 a plurality of packets.

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10 10. The program counter trace apparatus as recited in
11 claim 10 wherein the processor signals applied to the gate
12 unit include a program counter address, a periodic sync ID,
13 and a timing index.

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